IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A semiconductor device structure comprising:

a gate electrode including a vertical sidewall and a gate dielectric covering the vertical sidewall;

at least one semiconducting carbon nanotube extending vertically between opposite first and second ends at a location adjacent to said vertical sidewall of said gate electrode;

a first contact electrically coupled with said first end of said at least one semiconducting carbon nanotube; and

a second contact electrically coupled with said second end of said at least one semiconducting carbon nanotube.

2. (Currently Amended) The semiconductor device structure of claim 1 further comprising:

a catalyst pad electrically coupling said conductive carbon nanotube with said gate electrode, the catalyst pad participating in the synthesis of said ~~conductive~~ semiconducting carbon nanotube.

3. (Original) The semiconductor device structure of claim 1 wherein said at least one semiconducting carbon nanotube is a single-wall semiconducting carbon nanotube.

4. (Original) The semiconductor device structure of claim 1 further comprising:

a plurality of semiconducting carbon nanotubes extending vertically at a location adjacent to said vertical sidewall of said gate electrode.

5. (Currently Amended) The semiconductor device structure of claim 1 wherein said ~~source~~ first contact includes a catalyst pad characterized by a catalyst material effective for growing said at least one semiconducting carbon nanotube.

6. (Currently Amended) The semiconductor device structure of claim 5 wherein said first end of said at least one semiconducting carbon nanotube incorporates an electrical-conductivity enhancing substance diffused from said catalyst pad into said first end during ~~fabrication~~ growth.

7. (Original) The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said first contact and said gate electrode for electrically isolating said first contact from said gate electrode.

8. (Original) The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said second contact and said gate electrode for electrically isolating said second contact from said gate electrode.

9. (Withdrawn) The semiconductor device structure of claim 1 further comprising:

a third contact and at least one conductive carbon nanotube electrically coupling said gate electrode with said third contact.

10. (Original) The semiconductor device structure of claim 1 wherein said second contact includes a vertically-extending metal post electrically coupled with said second end of said at least one semiconducting carbon nanotube.

11. (Original) The semiconductor device structure of claim 10 wherein said second contact includes a conductive layer extending horizontally beneath said gate electrode for coupling said catalyst pad with said metal post.

12. (Withdrawn)The semiconductor device structure of claim 1 wherein said second contact includes at least one vertically-extending conductive carbon nanotube electrically coupled with said second end of said at least one semiconducting carbon nanotube.

13. (Withdrawn) The semiconductor device structure of claim 12 wherein said second contact includes a conductive layer extending horizontally beneath said gate electrode for coupling said catalyst pad with said at least one vertically-extending conductive carbon nanotube.

14. (Original) A circuit comprising an interconnected plurality of semiconductor device structures of claim 1 arranged in an array characterized by a plurality of rows and a plurality of columns.

15. (Original) The circuit of claim 14 wherein said plurality of semiconductor devices are interconnected as a memory circuit.

16. (Original) The circuit of claim 15 further comprising:

a plurality of word lines each electrically interconnecting said gate electrode of each of said plurality of semiconductor devices located in a corresponding one of said plurality of rows of said array; and

a plurality of bit lines each electrically interconnecting said second contact of each of said plurality of semiconductor devices located in a corresponding one of said plurality of columns of said array.

17. (Original) The circuit of claim 16 wherein each of said plurality of word lines comprises said gate electrode of said plurality of semiconductor devices.

18. (Original) The circuit of claim 16 wherein each of said plurality of bit lines comprises a conductive stripe electrically coupling said source of each of said plurality of semiconductor devices located in a corresponding one of said plurality of rows of said array.

19. (Original) The circuit of claim 14 further comprising:

a substrate carrying said plurality of semiconductor devices and characterized by a surface area viewed vertical to the substrate, said plurality of semiconductor devices separated by an open space that ranges from about 20 percent to about 50 percent of said surface area.

20. (Original) The circuit of claim 14 wherein said plurality of semiconductor devices are interconnected as a logic circuit.

21-33. (Cancelled)